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10/050,574	01/18/2002	Yu-Wei Chang	SUND 272	7051

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EXAMINER	
DAO, THUY CHAN	
ART UNIT	**PAPER NUMBER**
2192	

DATE MAILED: 06/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/050,574	CHANG, YU-WEI	
	Examiner	Art Unit	
	Thuy Dao	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 January 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the application filed January 18, 2002.

2. Claims 1-7 have been examined. Claims 1 and 5 are independent claims.

Priority

3. The application claims priority to a foreign patent application No. 90,102,690, Taiwan, R.O.C., filed February 7, 2001. The priority date considered for this application is February 7, 2001.

Oath / Declaration

4. The Office acknowledges receipt of a properly signed oath/declaration filed December 20, 2001.

Drawings

5. The drawings are objected to because the following informalities. Based on Specification, page 7, [0018], Fig. 2A needs an arrow pointing from 235 to 225.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet,

and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

6. The disclosure is objected to because of the following informalities:

The use of the trademarks Windows.TM. and MS-DOS.TM. (Microsoft Corporation), i.Link.TM. (Sony), and FireWire.TM. (Apple) have been noted in this application. It should be capitalized wherever it appears and be accompanied by the generic terminology.

Although the use of trademarks is permissible in patent applications, the proprietary nature of the marks should be respected and every effort made to prevent their use in any manner which might adversely affect their validity as trademarks.

Appropriate correction is required.

Claim Rejections – 35 USC §112, 2nd paragraph

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1 and 5 recite the limitation "said steps" in the third and second lines, respectively. There is insufficient antecedent basis for this limitation in the claims.

Claims 1 and 5 also recite the limitation "said status" in (f) and (e), respectively. There is insufficient antecedent basis for this limitation in the claims.

8. Bases on the specification, page 9, [0025], and the structure of claim 5(f), during examination, claim 1, section (f), the examiner is interpreting the limitations as:

(f) checking status of every interface card and debugging is performed if any error occurs; otherwise, said master interface card sending a plurality of check packets to the slave interface cards;

Claim Rejections – 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1, and 4-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,665,268 to Sato et. al (hereinafter "Sato"), and in view of US Patent No. 4,907,230 to Heller et. al (hereinafter "Heller").

Claim 1:

Sato discloses *a method for performing a load flow test among a plurality of* components (four preferred embodiments, related text and figures., e.g., Fig. 27), *said method comprising steps of:*

(a) initializing said components *and setting one of said* component *as a master* component *and said other* components *as slave* components (column 44, line 49 to column 46, line 43);

(b) said master component *initializing a plurality of communication protocol packets* (Fig. 27, SI1 and SI2, and related text, e.g., column 46, lines 45-54, " In FIG. 27, the processor element PE.sub.A (master program) generates the test information shown in FIG. 25 in step SI1, after which the process proceeds to step SI2. The test information shown in FIG. 25 is composed of 25 types of information including the packet ID (see FIG. 23), the source processor element, the destination processor element and the packet proper, and makes up packet information corresponding to the sets of the processor elements PE.sub.A to PE.sub.E (emphasis added))"

while said slave components *sending a plurality of first ready signals* (Fig. 27, PE, slave program side, START).

(c) said master component *sending said communication protocol packets to the slave* components *for responding to said first ready signals* (Fig. 27, SI4, SI5, and related text, e.g., column 47, lines 20-33, "In the case where the determination in step SI3 is YES, the processor element PE.sub.A (master program) proceeds to step SI5. In step SI5, the processor element PE.sub.A (master program) transmits the test information (including packets) to the processor elements PE.sub.B to PE.sub.E (slave programs) through the service processor 60 and then proceeds to step SI6.

In the case where the determination in step SI3 is NO, on the other hand, the processor element PE.sub.A (master program) proceeds to step SI4. In step SI4, the processor element PE.sub.A (master program) transmits the test information (including packets) to the processor elements PE.sub.B to PE.sub.E (slave programs) through the crossbar network unit 50, and then proceeds to step SI6");

(d) said slave component *sending a plurality of second ready signals for responding to the communication protocol packets sent by said master* component (Fig. 27, SI26-YES and related text, e.g., column 47, lines 42-45, "Upon receipt of the test information (including packets) from the processor element PE.sub.A (master program), the processor elements PE.sub.B to PE.sub.E determine the answer in step SI26 as YES, and proceed to step SI6";

(e) said master component *starting to perform said load flow test for responding to the second ready signals* (Fig. 27, SI7 and related text, e.g., column 47, lines 50-55, "In step SI7, the processor element PE.sub.A transmits the packet of packet ID 0 shown

in FIG. 25 to the destination processor element PE.sub.A, and then proceeds to step SI8, where it is determined whether a fault is detected at the time of transmission or not. In the case where this determination is NO, the process proceeds to step SI9";

(f) checking status of every component (Fig. 27, SI31 – SI33) *and*

debugging is performed if any error occurs (Fig. 27, SI37-SI39);

otherwise, said master component *sending a plurality of check packets to the slave* components (Fig. 27, SI9-YES);

(g) said slave components *sending a plurality of third ready signal for responding to the check packets* (Fig. 27, SI33-YES);

(h) said master component *sending a plurality of confirm signals to said slave* components *for responding to said third ready signals* (Fig. 27, SI14-YES); *and*

(i) said slave components *checking said test results for responding to said confirm signals* (Fig. 27, SI35 and related text, e.g., column 49, lines 44-49, "Also, when the determination in step SI32 or SI34 turns YES, the processor elements PE.sub.B to PE.sub.E proceed to step SI35. In step SI35, the processor elements PE.sub.B to PE.sub.E summarize the test result and proceed to step SI19. In step SI19, the processor elements PE.sub.A to PE.sub.E perform the synchronization process".

Sato does not explicitly disclose *a plurality of IEEE 1394 controllers, wherein said IEEE 1394 controllers are disposed on a plurality of interface cards individually.*

However, in an analogous art, Heller discloses a plurality of IEEE 1394 controllers, wherein said IEEE 1394 controllers are disposed on a plurality of interface cards individually (e.g., column 5, lines 29-45, "Another object of the invention is to detect faults in PCB's (printed circuit board) at the component level, while the components are in-circuit, without damage to the component.

Another object of the invention is to provide a tester that will test functionally at the board level and at the component level while the components are in-circuit. The invention detects open circuits and short circuits among components. The invention also tests analog and digital components at the component level. It tests IC's (integrated circuit) for open inputs, pins pulled to the power supply or to ground, and for shorts between inputs and outputs, and for internal IC failures.

Another object of the invention is to provide a system that will test a component under any set of operating conditions under which the component is specified to properly function" (emphasis added)).

Heller indeed discloses a method and an apparatus for testing electrical circuits, especially printed circuit boards containing a number of integrated circuit components (page 1, right column, lines 3-5), which include said interface cards and IEEE 1394 controllers.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the teachings of Sato and perform the load flow test among a plurality of IEEE 1394, which are disposed on a plurality of interface cards individually as taught by Heller. One would have been motivated to do so for generating tests for IC's that are not already included in the tester's IC library, learning the differences between a particular component while in circuit and while out of circuit, and acquiring and analyzing test data of PCBs as suggested by Heller (column 6, lines 25-44).

Claim 4:

The rejection of base claim 1 is incorporated. Sato does not explicitly disclose *said communication protocol packet is built by a command file mode, edit mode, or random mode.*

However, Heller further discloses communication protocol packet is built by a command file mode, edit mode, or random mode (column 17, lines 4-49, "In general, the application programs accept data from data files or from operator input to generate and execute test programs. In order to test a circuit, the invention requires the operator to connect the system to a physical circuit to be tested, to enter information about the normal operation and characteristics of that circuit, and to enter information about the normal operation and characteristics of each component...

If a test procedure for a known good PCB already is stored in BdFiles 1400 and information about its components is stored in ICInFiles 1600, the operator may test an unknown PCB by running BdTest 1000.

If no test procedures have yet been developed, but information about the board's components are stored in ICOutFiles 1500, the operator must run BdTestGen 1100 and BdSchLearn 1200 before running BdTest 1000. As explained below, BdTestGen 1100 prompts the operator to enter board layout and component data...").

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the teachings of Sato and Heller and build said communication protocol packet by a command file mode, edit mode, or random mode as taught by Heller. One would have been motivated to do so for being able to test different conditions: IC test models, functional testing, industry standard components, modified out-of-circuit IC test, known good PCBs, or components requiring more input information as suggested by Heller (column 17, lines 25-49).

Claim 5:

Sato discloses *a method for performing a load flow test between a master* component *and a slave* component (four preferred embodiments, related text and figures, e.g. Fig. 27), *said method comprising said steps of:*

(a) initializing said master component *and said slave* components *and building a test environment* (column 44, line 49 to column 46, line 43);

(b) said master component *initializing a communication protocol packet* (Fig. 27, SI1 and SI2, and related text, e.g., column 46, lines 45-54, " In FIG. 27, the processor element PE.sub.A (master program) generates the test information shown in FIG. 25 in step SI1, after which the process proceeds to step SI2. The test information shown in FIG. 25 is composed of 25 types of information including the packet ID (see FIG. 23), the source processor element, the destination processor element and the packet proper, and makes up packet information corresponding to the sets of the processor elements PE.sub.A to PE.sub.E (emphasis added))";

(c) said master component *sending said communication protocol packets for responding to a first ready signal from said slave* component (Fig. 27, SI4, SI5, and related text, e.g., column 47, lines 20-33, "In the case where the determination in step SI3 is YES, the processor element PE.sub.A (master program) proceeds to step SI5. In step SI5, the processor element PE.sub.A (master program) transmits the test information (including packets) to the processor elements PE.sub.B to PE.sub.E (slave programs) through the service processor 60 and then proceeds to step SI6.

In the case where the determination in step SI3 is NO, on the other hand, the processor element PE.sub.A (master program) proceeds to step SI4. In step SI4, the processor element PE.sub.A (master program) transmits the test information (including packets) to the processor elements PE.sub.B to PE.sub.E (slave programs) through the crossbar network unit 50, and then proceeds to step SI6");

(d) said slave component *sending said ready signal again for responding to said communication protocol packet* (Fig. 27, SI26-YES and related text, e.g., column 47, lines 42-45, "Upon receipt of the test information (including packets) from the processor element PE.sub.A (master program), the processor elements PE.sub.B to PE.sub.E determine the answer in step SI26 as YES, and proceed to step SI6");

(e) said master component *starting to perform said load flow test for responding to said ready signal in step (d)* (Fig. 27, SI7 and related text, e.g., column 47, lines 50-55, "In step SI7, the processor element PE.sub.A transmits the packet of packet ID 0 shown in FIG. 25 to the destination processor element PE.sub.A, and then proceeds to step SI8, where it is determined whether a fault is detected at the time of transmission or not. In the case where this determination is NO, the process proceeds to step SI9") *and*

checking said status of every component *for confirming whether an error occurs or not* (Fig. 27, SI31 – SI33).

(f) debugging if any error occurs in step (e) and rebuilding said environment (Fig. 27, SI37-SI39);

otherwise sending a check packet (Fig. 27, SI9-YES);

(g) said slave component *sending said ready signal again for responding to said check packet* (Fig. 27, SI33-YES);

(h) said master component *sending a confirm signal to said slave* component *for responding to said ready signal* (Fig. 27, SI14-YES)*;*

(i) said slave component *checking said test results for responding to said confirm signal* (Fig. 27, SI35 and related text, e.g., column 49, lines 44-49, "Also, when the determination in step SI32 or SI34 turns YES, the processor elements PE.sub.B to PE.sub.E proceed to step SI35. In step SI35, the processor elements PE.sub.B to PE.sub.E summarize the test result and proceed to step SI19. In step SI19, the processor elements PE.sub.A to PE.sub.E perform the synchronization process")*; and*

(j) said master component *sending an instruct signal for deciding either exiting or resuming* (Fig. 27, SI25-END (exiting), SI24-NO (resuming), and related text, e.g., column 49 line 62 to column 50 line 8).

Sato does not explicitly disclose *a master interface card and a slave interface card.*

However, in an analogous art, Heller discloses a method for performing a test between a master interface card and a slave interface card (e.g., column 5, lines 29-45, "Another object of the invention is to detect faults in PCB's (printed circuit board) at the component level, while the components are in-circuit, without damage to the component.

Another object of the invention is to provide a tester that will test functionally at the board level and at the component level while the components are in-circuit. The

invention detects open circuits and short circuits among components. The invention also tests analog and digital components at the component level. It tests IC's (integrated circuit) for open inputs, pins pulled to the power supply or to ground, and for shorts between inputs and outputs, and for internal IC failures.

Another object of the invention is to provide a system that will test a component under any set of operating conditions under which the component is specified to properly function" (emphasis added)").

Heller indeed discloses a method and an apparatus for testing electrical circuits, especially printed circuit boards containing a number of integrated circuit components (page 1, right column, lines 3-5), which include said interface cards and IEEE 1394 controllers.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the load flow test taught by Sato and perform said test between a master interface card and a slave interface card as taught by Heller. One would have been motivated to do so for generating tests for IC's that are not already included in the tester's IC library, learning the differences between a particular component while in circuit and while out of circuit, and acquiring and analyzing test data of PCBs as suggested by Heller (column 6, lines 25-44).

Claim 6:

The rejection of base claim 5 is incorporated. Sato does not explicitly disclose *said test environment is Microsoft Disk Operating System (MS-DOS).*

However, Heller also discloses "FIG. 10 is a flowchart showing the relationship between the operating system, the operator interface, and the system programming. The operating system in the preferred embodiment is MS-DOS and can be used with standard BASIC commands" (column 16, lines 55-59).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the teachings of Sato and Heller and let the test environment be Microsoft Disk Operating System as taught by Heller. One would have been motivated to do so for permitting the load flow test to be used with a standard host system, and allowing the said host system to use off-the-shelf applications programs such as for database and word processing as suggested by Heller (column 16, lines 59-63).

Claim 7:

The rejection of base claim 5 is incorporated. Claim 7 recites the same limitations as those of claim 4, wherein all claimed limitations have been addressed and/or set forth above. Therefore, as the combined references teach all of the limitations of claim 4, they also teach all of the limitations of claim 7.

11. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sato and Heller as applied to claim 1 above, and further in view of US Patent No. 6,775,824 to Osborne et. al (hereinafter "Osborne").

Claim 2:

The rejection of base claim 1 is incorporated. Sato and Heller disclose *said step (a) further comprising said steps of:*

(a1) initializing said interface cards (column 13, lines 12-26, e.g., "The load test program referred to herein indicates the master program MP and the slave programs SP.sub.0 to SP.sub.3 shown in FIG. 4. The master program MP and the slave programs SP.sub.0 to SP.sub.3 are in the master-slave relation to each other. The master program MP is for controlling the execution of the slave programs SP.sub.0 to SP.sub.3 and stored in the memory 14.sub.0 (see FIG. 1) of the process or element PE.sub.0... The slave programs SP.sub.0 to SP.sub.3, on the other hand, are stored in the memories 14.sub.0 to 14.sub.3 of the processor elements PE.sub.0 to PE.sub.3, respectively, and used for conducting a load test under the control of the master program MP. These slave programs SP.sub.0 to SP.sub.3 are executed by the CPUs 13.sub.0 to 13.sub.3, respectively");

(a2) waiting an operating system of said host being ready (Fig. 6, master program-START)*; and*

(a3) building a test environment for communicating said interface cards with one another (Fig. 6, SA1, Synchronization Processing).

Sato and Heller do not explicitly disclose the interface cards are placed on at least one host.

However, in an analogous art of a system for testing middleware of applications, Osborne discloses the interface cards are placed on at least one host in the N-tiered model (column 3, lines 30-37, e.g., "With the foregoing background in mind, it is an object of the invention to provide testing tools to facilitate load based testing of N-tiered applications.

It is also an object to provide automatic testing.

The foregoing and other objects are achieved by a test system that generates test code for components of an application under test using interface information about the components").

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the teachings of Sato and Heller and perform the load flow test on said interface cards placed in at least one host as taught by Osborne. One would have been motivated to do so for being able to perform a mass load flow testing as suggested by Osborne (column 1, lines 59-65, "One advancement in the N-tiered model is that the middleware is very likely to be componentized and is very likely to be

written to a component standard so that it will easily integrate with software at other tiers").

Claim 3:

The rejection of base claim 2 is incorporated. Claim 3 recites the same limitations as those of claim 6, wherein all claimed limitations have been addressed and/or set forth above. Therefore, as the combined references teach all of the limitations of claim 6, they also teach all of the limitations of claim 3.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Wikipedia Encyclopedia (from website: answers.com): "Controllers, when used in computing and especially in computer hardware, often occur when interfacing with peripherals".

Microsoft Computer Dictionary, Fifth Edition, page 18, interface card is defined as "a printed circuit board that enables a personal computer to use a peripheral device... See also controller, expansion board, network adapter...".

13. Any inquiry concerning this communication should be directed to examiner Thuy Dao (Twee), whose telephone is (571) 272 8570. The examiner can normally be reached on Monday – Friday from 6:30AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam, can be reached at (571) 272 3695.

The fax phone number for the organization where this application or proceeding is assigned is (703) 872 9306.

Any inquiry of a general nature of relating to the status of this application or proceeding should be directed to the TC 2100 Group receptionist whose telephone number is (571) 272 2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

T. Dao

WEI Y. ZHEN
PRIMARY EXAMINER